UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,203	09/14/2000	Alnoor M. Shivji	005100.P008	1520

47827 7590 06/21/2005

BIRCH, STEWART, KOLASCH & BIRCH LLP
PO BOX 747
8110 GATEHOUSE ROAD, STE 500 EAST
FALLS CHURCH, VA 22040-0747

EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/661,203	SHIVJI ET AL.	
	Examiner	Art Unit	
	Ian N. Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,8-10,12,13 and 16-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23* is/are allowed.

6)☒ Claim(s) *1,2,4,5,8-10,12,13,16-22 and 24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claim rejection, on claims 1,9,17 under double patenting are withdrawn since they are being amended accordingly.

2. Claim rejection, on claims 1,2,4,5,8-10,12,13,16 and 24-26 under 35 USC § 112 second paragraph are withdrawn since they are being amended accordingly.

3. Previously referred and cited Upp reference (US 5,040,170) is incorporated in PTO-892, which is attached to this final official office action.

4. Claims 1,2,4,5,8-10,12,13,16-22, and 24-29 are rejected by the new ground(s) of rejection necessitated by the amendment.

Claim Objections

5. Claims 1, 9, 17 are objected to because of the following informalities:

Claim 1 recites, "**an** application specific integrated circuit (ASIC) on the cross connect card for performing serial-to-parallel conversion...performing switching functions...performing parallel-to-serial conversion..." in lines 9-17, which is not described in the specification. Per FIG, 8 and specification page 20-21, **three** ASICs are performing these three functions (i.e. HISSA 825 performing serial-to-parallel conversion, TISSA 830 switching functions, and HISSA 835 performing parallel-to-serial conversion).

Claims 9 and 17 are also rejected for the same reason as stated in claim 1 above.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1,4,5,6,8,9,12,13,16-21 and 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gingell (U.S. 5,497,363) in view of Laor (US006424649B1).

Regarding Claim 9, Gingell discloses an apparatus (see FIG. 2, add/drop multiplexer setup (note that FIG. 2 is the combination of FIG. 2A and 2B); or see FIG. 3, a LCX-150 Add/drop multiplexer shelf) comprising:

means for receiving network data in a first format (see FIG. 2; DS1 or DS0s asynchronous format) via a first card (see FIG. 2, DMI-1 or DMI-2, Drop Module Interface; see FIG. 3, DMI card 34,36 or 38; note that each DMI card receives DS1/DS0 data) coupled to a first network (see FIG. 2, the DS0 or DS1 asynchronous network; see col. 4, lines 12-40; col. 7, lines 25-40);

means for converting the data to a synchronous optical network (SONET/SDH) format (see FIG. 2A, SONET formatter 92 of DMI-1 and see FIG. 2A, VT formatter 104/106 of DMI-2; see col. 5, lines 13-50; the received DS1 and DS0 are converted into SONET formatted signal STS1);

means for transmitting the SONET/SDH formatted data (see FIG. 2, STS1 signal) from the first card as a first set one or more serial data signals (see FIG. 2A, each STS1 signal is serially transmitted by the DMI card; see col. 7, lines 35-45) to a cross-connect card (see FIG. 2A, VSCC 30, cross-connect) via a backplane (see FIG. 3, a backplane of the ADM shelf; see FIG. 2A, the combined system of data buses 26,28,32, 56, 40,42,44 forms the backplane; see col. 4, lines 9-45; note that STS1 signal from each DMI card is serially transmitted to VSCC card via a backplane);

means for using an application specific integrated circuit (ASIC) on the cross-connect card (see FIG. 2A, VTCC ASIC 88) to

perform switching function on the SONET/SDH formatted data in the first set of one or more serial data (see col. 5, lines 5-25; perform on serial data from DMI card);

perform switching function on the SONET/SDH formatted data in the first set of one or more serial data (see col. 5, lines 5-25; perform on serial data to OC-3 card);

performing switching functions on the SONET/SDH formatted data at the cross-connect card (see col. 4, lines 1-13; note that SONET formatted data (i.e. VTs and STSs) are switched/cross-connected in the VSCC ASIC);

means for transmitting the SONET/SDH formatted data at the cross-connect card (see FIG. 2A, STS1 signal is transmitted towards high speed east/west OC-3 card by VSCC card; see col. 3, lines 65 to col. 4, lines 5);

means for transmitting the SONET/SDH formatted data as the second set of one or more serial data signals to a second card via backplane (see FIG. 2, OC-3 high speed interface 22, 24; see FIG. 3, OC-3 East 22 or West 24 card; see col. 3, lines 60 to col. 4, lines 1, 52-67, see col. 5, lines 1-6; note that STS1 multiplexed signal is serially transmitted toward OC-3 high speed card via a backplane/bus 26 or 28; note that STS1 serial signal contains multiplexed DS1 and DS0 signals), the second card being coupled to a second network (see FIG. 2, OC-3 High speed card connects to high speed synchronous SONET network; see col. 3, lines 44-64);

means for converting the SONET/SDH formatted data to a second format (see FIG. 2, OC3 optical signal format 12, 14; see col. 4, lines 64 to col. 5, lines 6; note that ASICs in the OC-3 card converts between electrical STS-1 and optical signal format OC-3);

means for transmitting the data in the second format to the second network via the second card (see FIG. 2, OC-3 optical signal 12,14 is transmitted via OC-3 high speed card 22,24 to the synchronous high speed SONET network; see col. 3, lines 40-64).

wherein the backplane utilizes a common signaling scheme to communicatively connect the first card, second card, and cross-connect card (see FIG. 3, a backplane in the ADM shelf houses/connects OC3 cards 22,24, VSCC card 30, and DMI card 34,36,38; see FIG. 2, the data bus 26,32,28, 56, see col. 4, lines 1-20; note that it is inherit that the backplane/combined system of buses must

utilize the common signaling/protocol in order perform inter-shelf communication between OC-3, VSCC and DMI cards).

Gingell does not explicitly disclose performing serial-to-parallel conversion and parallel-to-serial conversion. However, Laor teaches the cross connect card (see FIG. 2, X-Connect 110) for:

perform serial-to-parallel conversion (see FIG. 2, Serial parallel converter 210) on the SONET/SDH formatted data (see col. 2, lines 45-50, 59-65; SONET format) in the first set of one or more serial data signals (see FIG. 2, serial signals received from interface card 130 (in parallel serial converter 200); see col. 3, lines 50-57; see col. 4, lines 10-15),

perform switching functions on the SONET/SDH formatted data at the cross-connect card (see FIG. 2, cross bar switch 220; see col. 4, lines 35-46), and

perform parallel-to-serial conversion (see FIG. 2, parallel serial converter 230) on the switched SONET/SDH formatted data to generate a second set of one or more serial data signals (see FIG. 2, serial signals to interface card 150 (in serial parallel converter 240); see col. 4, lines 40 to col. 5, lines 12. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide serial-to-parallel conversion and parallel-to-serial conversion, as taught by Laor in the system of Gingell, so that it would rapidly synchronously and serially switching large amount of data and accrues no synchronization delay; see Laor col. 1, line 40-60.

Regarding Claim 1, the method claim, which has substantially disclosed all the limitations of the respective apparatus claim 9. Therefore, it is subjected to the same rejection.

Regarding Claim 17, the system claim, which has substantially disclosed all the limitations of the respective apparatus claim 9. Therefore, it is subjected to the same rejection.

Regarding Claim 4, the combined system of Gingell and Laor discloses all claimed limitations. Gingell discloses wherein each of the first and second sets of one or more serial data signals are transmitted via the backplane as a differential pair (see FIG. 2A, two lines on bus 26, 28 or 32; see col. 4, lines 1-27; note that each serial/multiplexed STS-1 signal is transmitted through backplane/combined system of the buses in different/differential pair.) Laor also discloses the first and second sets of one or more serial data signals are transmitted as described above in claim 1.

Regarding Claim 5, Gingell discloses wherein the data in the second format comprises an aggregation of multiple data signals in the first format (see FIG. 2A, 28 ASYNC DS1 in DMI card 34,36,38; an STS1 signal 32 from each DMI card; ASICs STS-3 (72,76,78,64) in OC-3 card 22; see col. 3, lines 60 to col. 5, lines 13; note that 28 DS1 encapsulated into 28 VT1.5 containers and then multiplexed into an STS-1 in each DMI card. Three STS-1s from three DMI cards are multiplexed into an STS-3, which is converted into optical format OC-3. Thus, optical signal OC-3 comprises an aggregated/multiplexed DS1 signals).

Regarding Claim 8, Gingell discloses wherein the SONET/SDH formatted data according to one of STS-1, STS-3, STS-12, STS-48 and STS-192 protocols (see FIG. 2A, STS-3 and STS-1 format; and col. 1, lines 65-67, see col. 4, lines 67).

Regarding Claim 12, the claim, which has substantially disclosed all the limitations of the respective apparatus claim 4. Therefore, it is subjected to the same rejection.

Regarding Claim 13, the claim, which has substantially disclosed all the limitations of the respective apparatus claim 5. Therefore, it is subjected to the same rejection.

Regarding Claim 16, the claim, which has substantially disclosed all the limitations of the respective apparatus claim 8. Therefore, it is subjected to the same rejection.

Regarding claim 18, Gingell discloses wherein the first (see FIG. 2A, DMI card 34 comprising SONET formatter 92 (SFMT ASIC)) and second card each include an application specific integrated circuit (see FIG. 2A, OC-3 card comprising a combined system of ASIC 76,78 and 64) configured to perform parallel-to-serial conversion (see FIG. 2A, ASIC 92 of DMI-1 card multiplexes (i.e. parallel-to-serial conversion) 28 DS1 signals into an SONET format STS-1 signal; and see FIG. 2A, the combined ASIC 76,78,64 of OC-3 card multiplexes three SONET format STS-1 signals into an STS-3/OC-3 signal) and serial-to-parallel conversion on data in the SONET/SDH format (see FIG. 2A, the combined ASIC 76,78,64 of OC-3 card demultiplexes (i.e. serial-to-parallel) an OC-3/STS-3 signals into three SONET

format STS-1 signals; and see FIG. 2A, ASIC 92 of DMI-1 card demultiplexes an STS-1 signal into 28 DS1 signals; see col. 4, lines 64 to col. 5, lines 35; see col. 1, lines 44 to col. 2, lines 9).

Regarding claim 19, Gingell further teaches wherein perform parallel-to-serial conversion on the data in the SONET/SDH format (see FIG. 2A, ASIC 92 multiplexes 28 DS1s into an STS1), thereby making the data suitable for transmission to the cross-connect card via the backplane (see FIG. 2A, STS1 via backplane/bus 32 towards VSCC 30; note that 28 DS1 must be multiplexed into an SONET STS-1 in order to transmit towards VSCC via backplane for switching; see col. 4, lines 64 to col. 5, lines 35; see col. 1, lines 44 to col. 2, lines 9).

Regarding claim 20, Gingell further teaches wherein perform serial-to-parallel conversion on the data in the SONET/SDH format (see FIG. 2A, ASIC 92 demultiplexes an STS1 into 28 DS1), the data being received from the cross-connect card via the backplane (see FIG. 2A, an STS1 signal is received from VSCC 30 via backplane/bus 32; see col. 4, lines 64 to col. 5, lines 35; see col. 1, lines 44 to col. 2, lines 9).

Regarding claim 21, Gingell further discloses the cross connect card includes an application specific integrated circuit (ASIC) (see FIG. 2A, VTCC ASIC 88) configured to perform the switching functions on the data in the SONET/SDH format (see col. 5, lines 6-13; VTCC ASIC 88 performs VT/STS1 cross connect switching between lines 26,28, and 32).

Regarding claim 24, Gingell further discloses wherein the common signaling scheme utilizes differential pair signaling (see FIG. 2A, two lines on bus 26, 28 or 32; see col. 4, lines 1-27; note that each serial/multiplexed STS-1 signal is transmitted through backplane/combined system of the buses in different/differential pair) at a predetermined frequency (note that since ASIC 92, 88, 64 process the STS-1 signal rate (i.e. electrical format, 51.84 Mb/s), it is inherent that they must be operate in predefined STS-1 frequency 51 MHz).

Regarding claim 25, Gingell further discloses wherein the backplane includes a plurality of card slots (see FIG. 3, card slots in ADM shelf 50), the first and second cards respective ones of the plurality of card slots (see FIG. OC3 cards are plugged into the high-speed slots; and DMI being plugged into DMI slots; see col. 5, lines 59 to col. 6, lines 4).

Regarding claim 26, Gingell further discloses plugging a third card (see FIG. 2B, DMI-2 38; see FIG. 3, DMI card for drop 3) into an used one of the plurality of card slots (see FIG. 3, DMI-2 card is plug into unused drop 3 slot), the third card being coupled to a third network (see FIG. 2, DMI-2 38 is connected to DS0 network) and

using the cross-connect card to perform switching functions on data to be transmitted (see FIG. 2A, VSCC 30 also performs cross connection for STS1 signal received from DMI-2 36) between the third network (see FIG. 2A, DS0 network) and at least one of the first and second networks (see FIG. 2A, OC-3 high speed optical network); see col. 20-50; see col. 5, lines 36 to col. 6, lines 5).

Regarding Claim 27, the claim, which has substantially disclosed all the limitations of the respective claim 24. Therefore, it is subjected to the same rejection.

Regarding Claim 28, the claim, which has substantially disclosed all the limitations of the respective claim 25. Therefore, it is subjected to the same rejection.

Regarding Claim 29, the claim, which has substantially disclosed all the limitations of the respective claim 26. Therefore, it is subjected to the same rejection.

8. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gingell in view of Sahlman (U.S. 6,693,902).

Regarding claim 2, Gingell discloses wherein performing switching functions on the SONET/SDH formatted data comprises performing time switching (see col. 5, line 5-12; see col. 9, lines 39-65; note that cross connect between SONET STS1s is performed according to cross connecting or interchanging time slots).

Gingell does not explicitly disclose space switching.

However, the above-mentioned claimed limitations are taught by Sahlman. In particular, Sahlman teaches wherein performing switching functions (see FIG. 1, cross connect switch) on the SONET/SDH formatted data (see FIG. 1, STM-1 signals) comprises performing time switching (see FIG. 1 time switches T) and space switching (see FIG. 1, Space Switch S; see col. 4, line 62 to col. 5, lines 55).

In view of this, having the system of Gingell and then given the teaching of Sahlman, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Gingell, by providing a time

and space switching, as taught by Sahlman. The motivation to combine is to obtain the advantages/benefits taught by Sahlman since Sahlman states at col. 2, line 40-60 that such modification would reduce the number of required space switch modules in large cross connects which will reduce the need for the quadric expanding.

Regarding Claim 10, the claim, which has substantially disclosed all the limitations of the respective claim 2. Therefore, it is subjected to the same rejection.

9. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gingell in view of Laor, as discloses in above claim 17, and further in view of Upp (U.S. 5,040,170).

Regarding claim 22, Gingell discloses wherein the cross-connect card includes a first application specific integrated circuit (ASIC) (see FIG. 2A, VTCC ASIC 88) the circuit being configured to perform conversion on data in the SONET/SDH format (see col. 5, lines 6-13; VTCC ASIC 88 performs VT/STS1 cross connect switching between lines 26,28, and 32 in the STS1 format). Laor discloses wherein the cross connect cards contains a first circuit being configured to perform parallel-to-serial and a second circuit being configured to perform serial-to-parallel conversion as described above in claim 17.

Neither Gingell nor Laor explicitly discloses the second application specific integrated circuit (ASIC). However, Upp discloses a first circuit (see Upp FIG. 1, VTX, 900) being configured to perform parallel-to-serial conversion (see Upp FIG. 1,

VTX 900 is designed/configured to receive parallel inputs from SBI 600 and transmitted into a serial output towards WBX 900 in SONET format) and serial-to-parallel conversion (see Upp FIG. 1, VTX 900 is designed/configured to receive a serial input from WBX and transmitted into the parallel outputs toward SBI 600 in SONET format); and

the second application specific integrated circuit (ASIC) (see Upp col. 15, lines 35-51; WBX includes a application specific (i.e. CMOS) integrated circuit) being configured to perform parallel-to-serial conversion (see Upp FIG. 1, WBX 900 is designed/configured to receive the parallel inputs from SPT 400 (i.e. STS-1) and transmitted a serial output towards VTX in SONET format) and serial-to-parallel conversion on data in the SONET/SDH format (see Upp FIG. 1, WBX 900 is designed/configured to receive a serial input from VTX and transmitted the parallel outputs toward SPT 400 (i.e. STS-1) in SONET format); see col. 7, lines 21-60.

In view of this, having the combined system of Gingell and Laor then given the teaching of Upp, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Gingell and Laor, by providing second WBX integrated circuit for the cross connect/switch matrix, as taught by Upp. The motivation to combine is to obtain the advantages/benefits taught by Upp since Upp states at col. 7, line 38-60 that such modification would provide wide band cross-connect switching and virtual tributary cross-connect switching capabilities in the network and provide simultaneous switching of digital signals having different data rates.

Allowable Subject Matter

10. Claim 23 is allowed.

Response to Arguments

11. Applicant's arguments with respect to claims 1,2,4,5,8-10,12,13 and 16-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
6/10/05

BOB PHUNKULH
PRIMARY EXAMINER